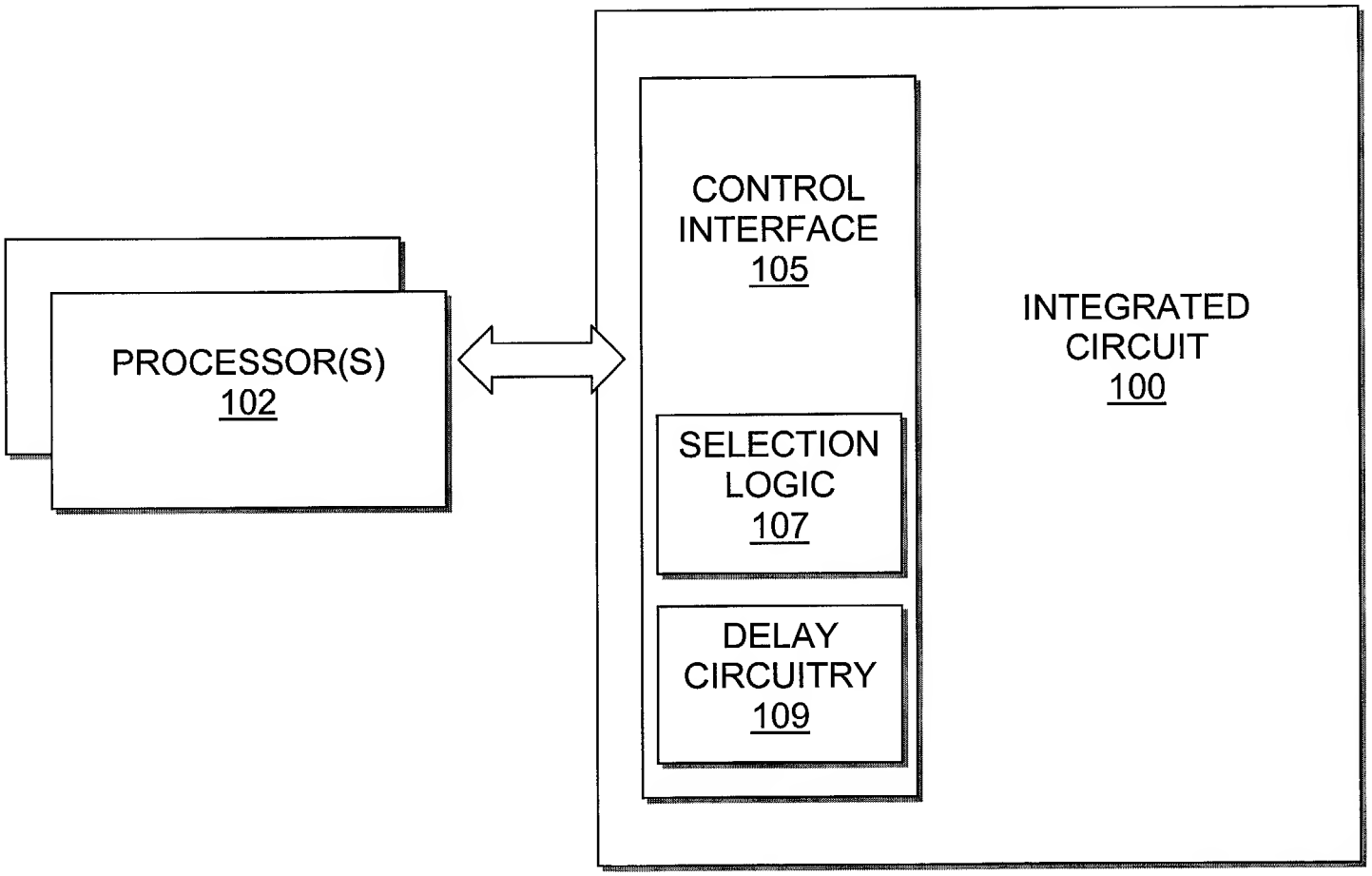
PROCESSOR(S)
102
CONTROL
INTERFACE
105
SELECTION
LOGIC
107
DELAY
CIRCUITRY
109
INTEGRATED
CIRCUIT
100

FIG. 1

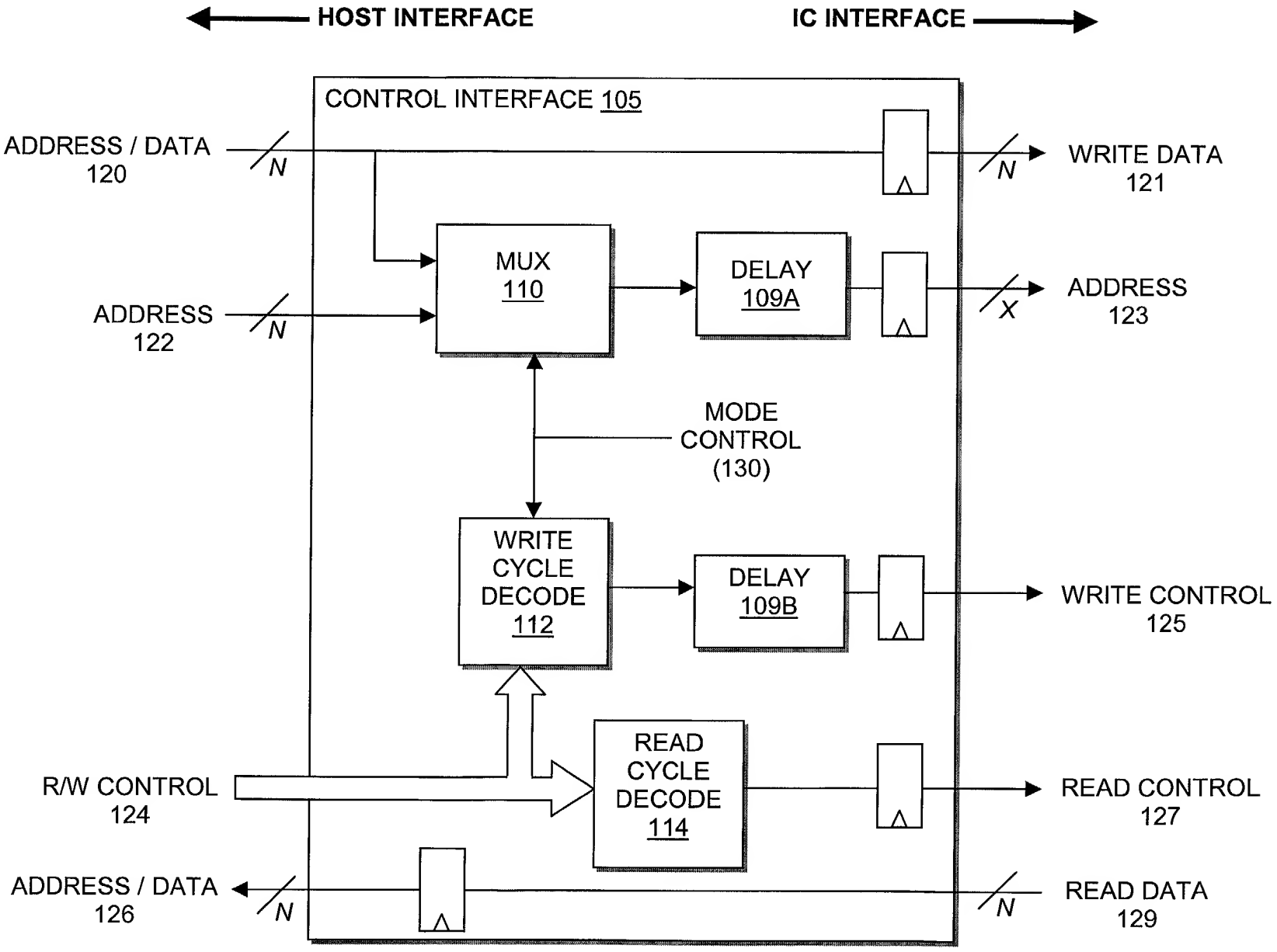
HOST INTERFACE
IC INTERFACE
CONTROL INTERFACE 105
ADDRESS / DATA
120
N
WRITE DATA
121
MUX
110
DELAY
109A
ADDRESS
122
ADDRESS
123
X
MODE
CONTROL
(130)
WRITE
CYCLE
DECODE
112
DELAY
109B
WRITE CONTROL
125
READ
CYCLE
DECODE
114
R/W CONTROL
124
READ CONTROL
127
ADDRESS / DATA
126
READ DATA
129

FIG. 2

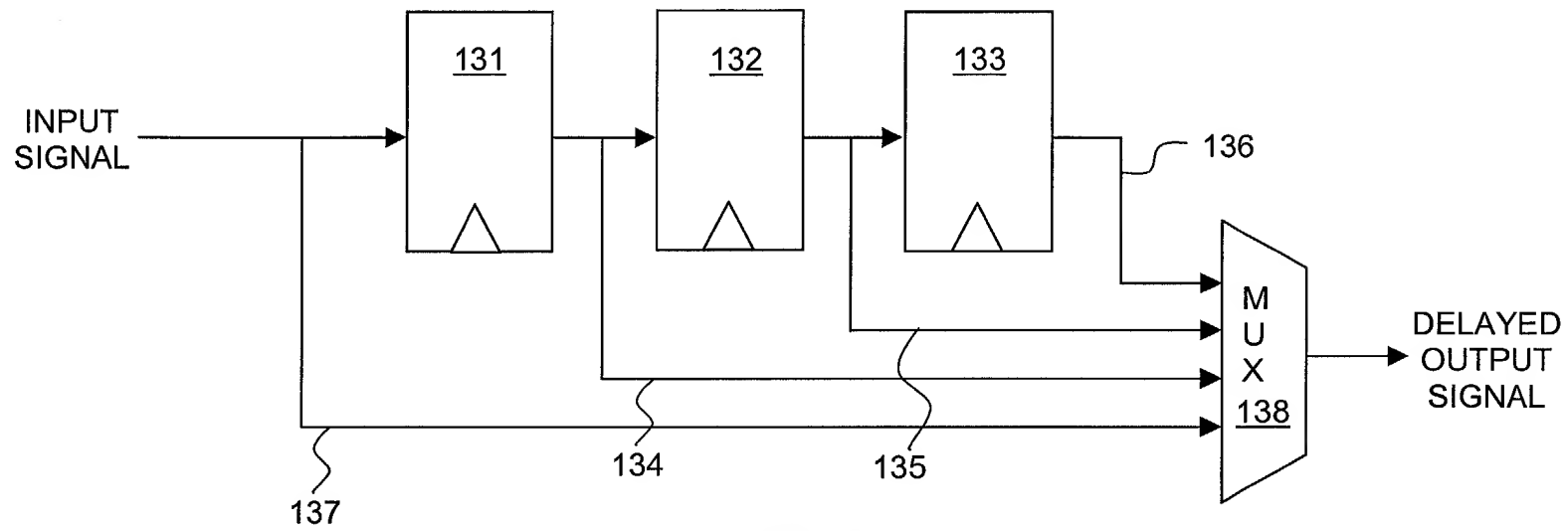
INPUT SIGNAL
131
132
133
136
M U X 138
DELAYED OUTPUT SIGNAL
134
135
137

FIG. 3

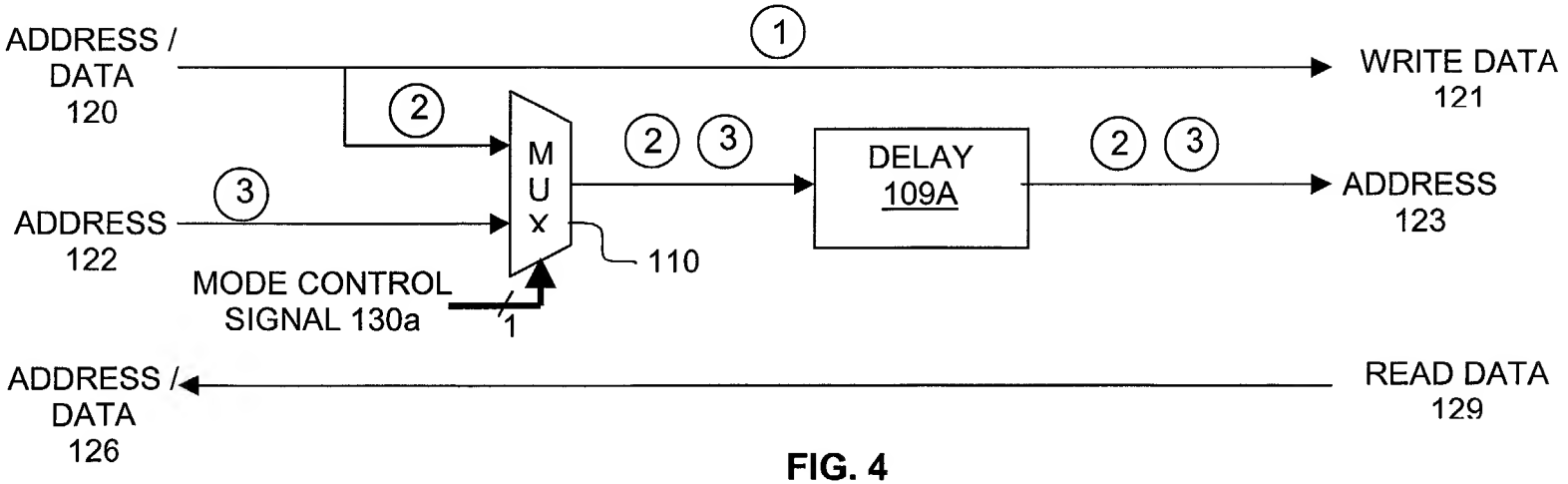
ADDRESS / DATA 120
1
WRITE DATA 121
2
2 3
2 3
M U x
DELAY 109A
3
ADDRESS 122
ADDRESS 123
110
MODE CONTROL SIGNAL 130a
1
ADDRESS / DATA 126
READ DATA 129

FIG. 4

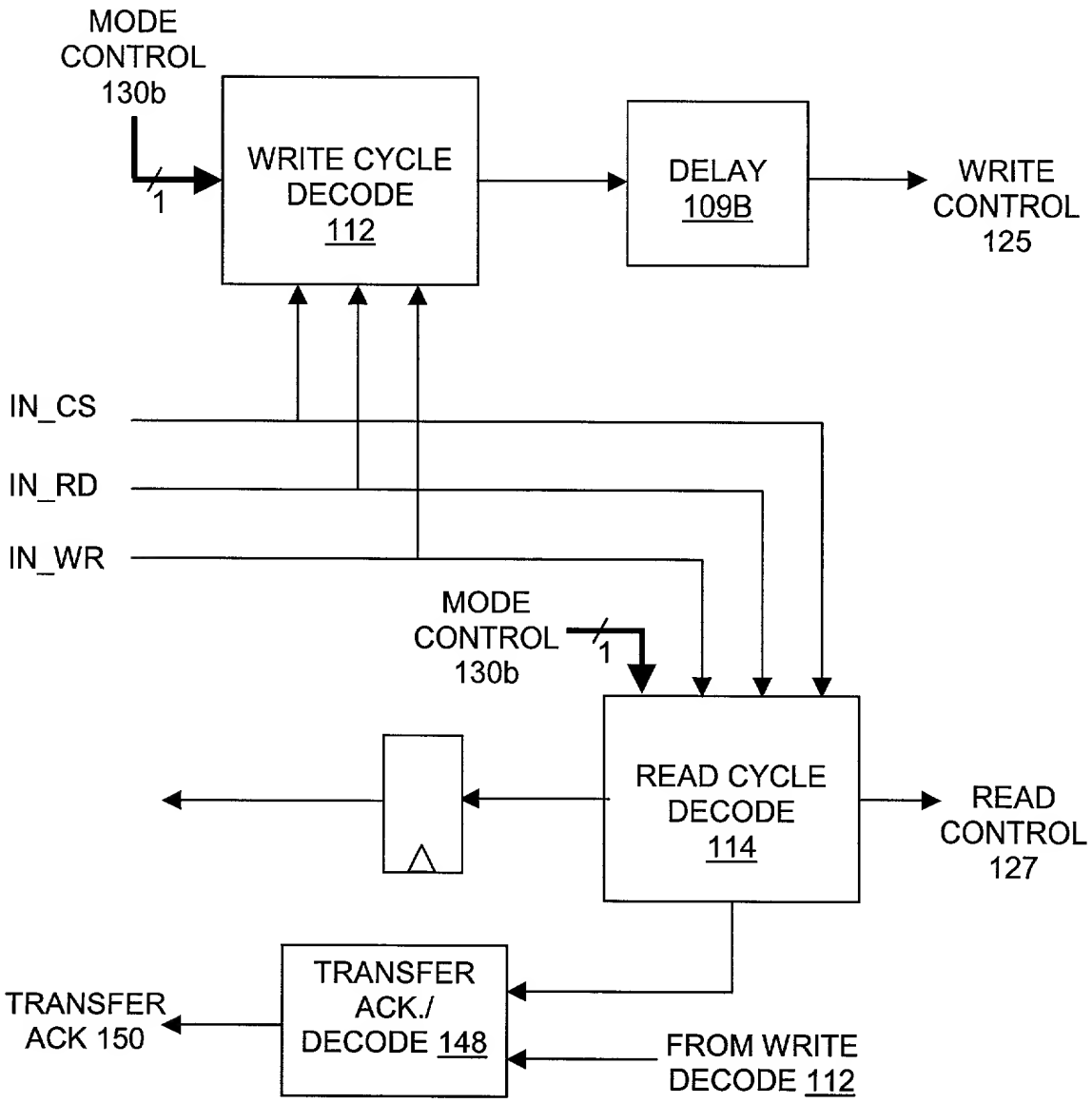
MODE
CONTROL
130b
1
WRITE CYCLE
DECODE
112
DELAY
109B
WRITE
CONTROL
125
IN_CS
IN_RD
IN_WR
MODE
CONTROL
130b
1
READ CYCLE
DECODE
114
READ
CONTROL
127
TRANSFER
ACK./
DECODE 148
TRANSFER
ACK 150
FROM WRITE
DECODE 112

FIG. 5

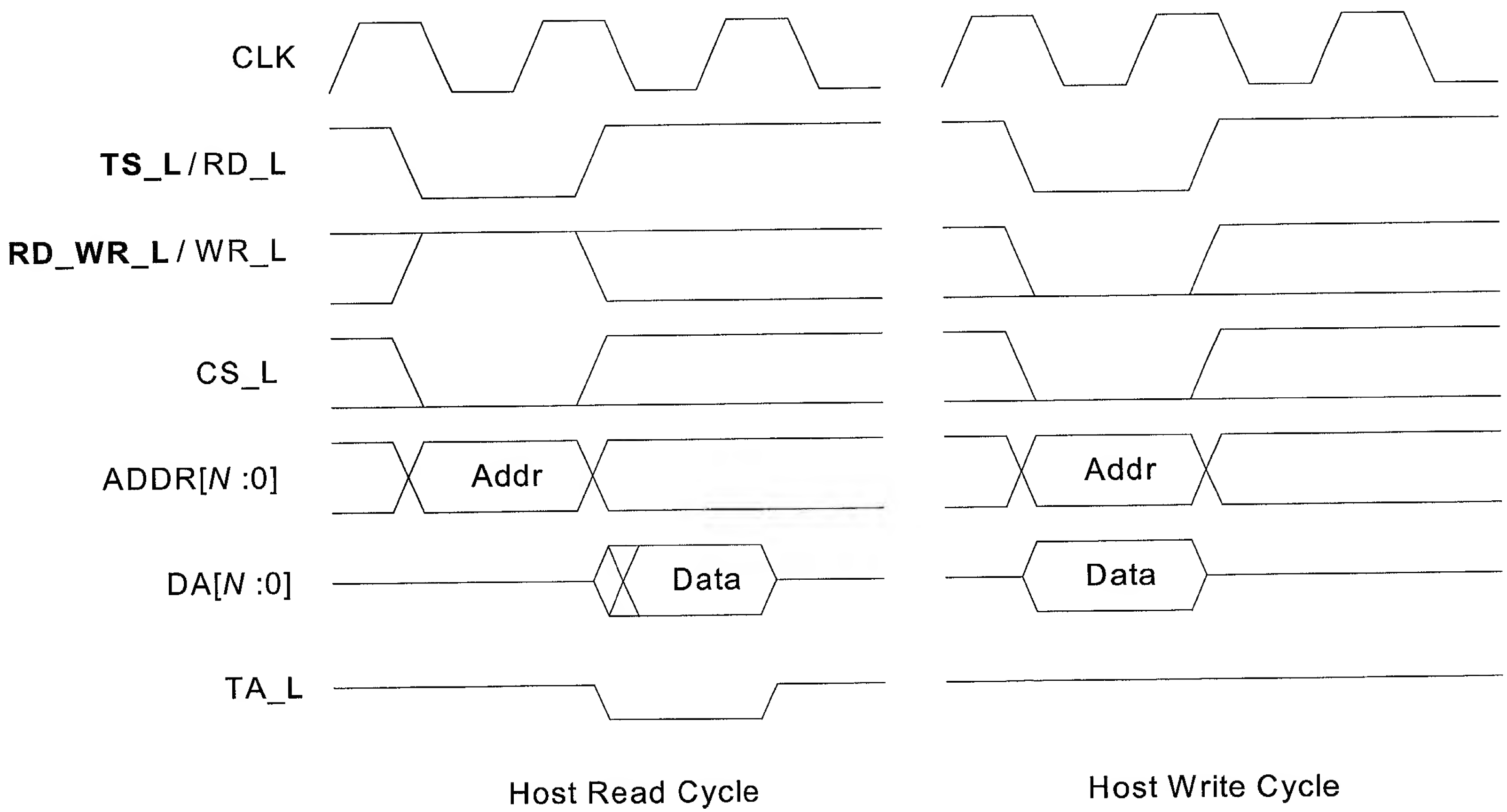
CLK
TS_L / RD_L
RD_WR_L / WR_L
CS_L
ADDR[N :0]
DA[N :0]
TA_L
Addr
Data
Addr
Data
Host Read Cycle
Host Write Cycle

FIG. 6A

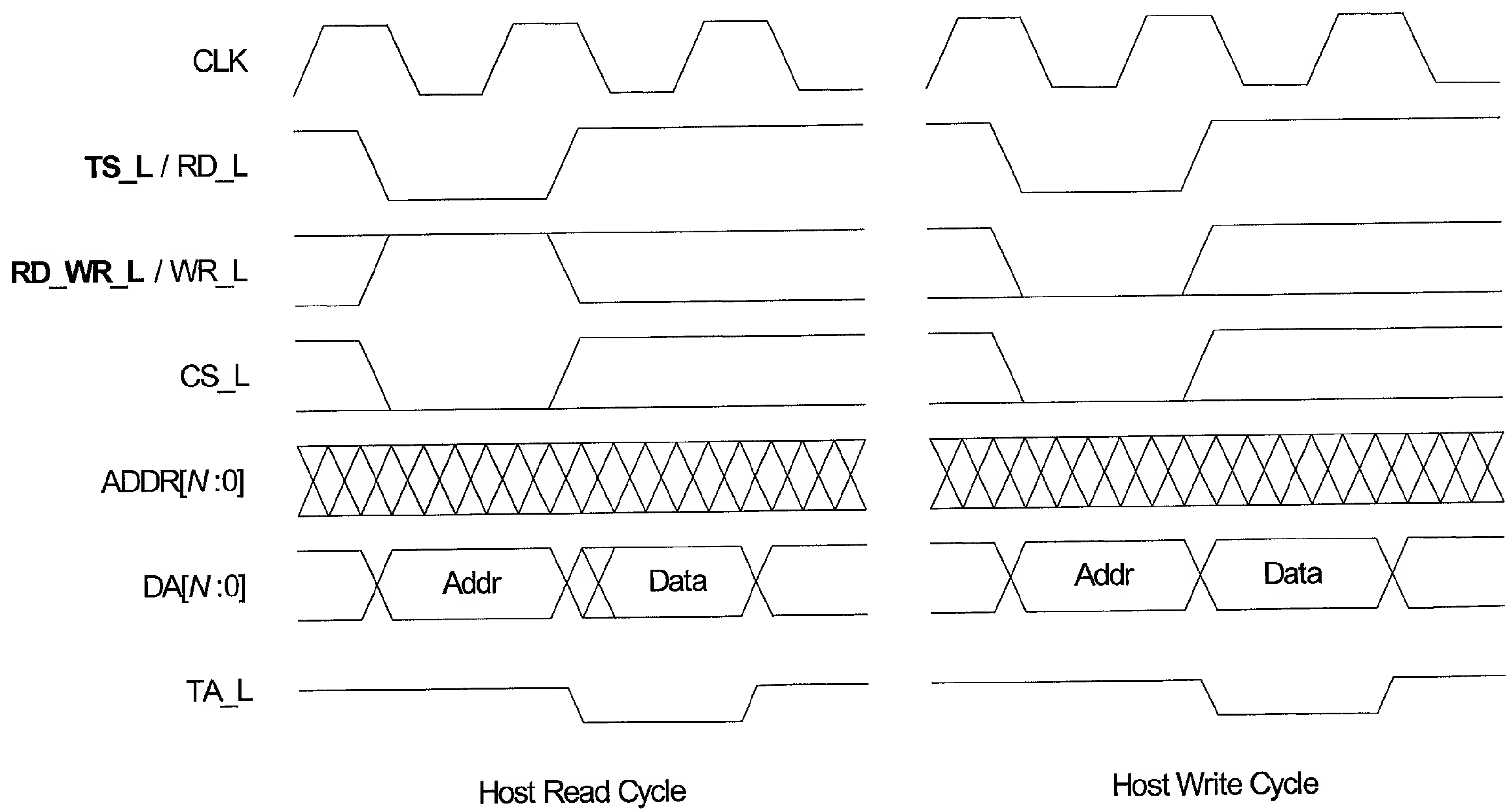
CLK
TS_L / RD_L
RD_WR_L / WR_L
CS_L
ADDR[N:0]
DA[N:0]
Addr
Data
Addr
Data
TA_L
Host Read Cycle
Host Write Cycle

FIG. 6B

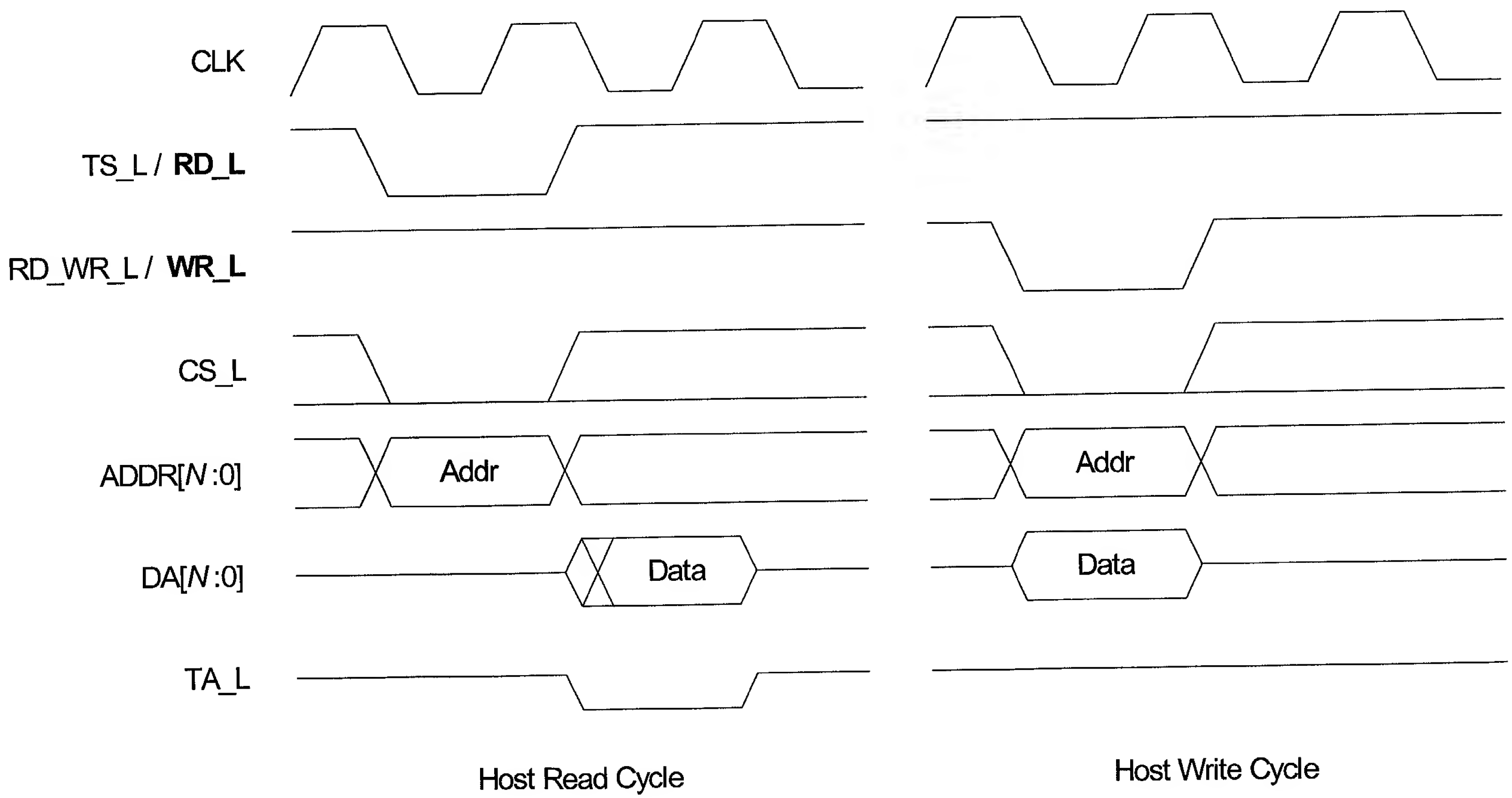
CLK
TS_L / RD_L
RD_WR_L / WR_L
CS_L
ADDR[N:0]
DA[N:0]
TA_L
Addr
Data
Addr
Data
Host Read Cycle
Host Write Cycle

FIG. 6C

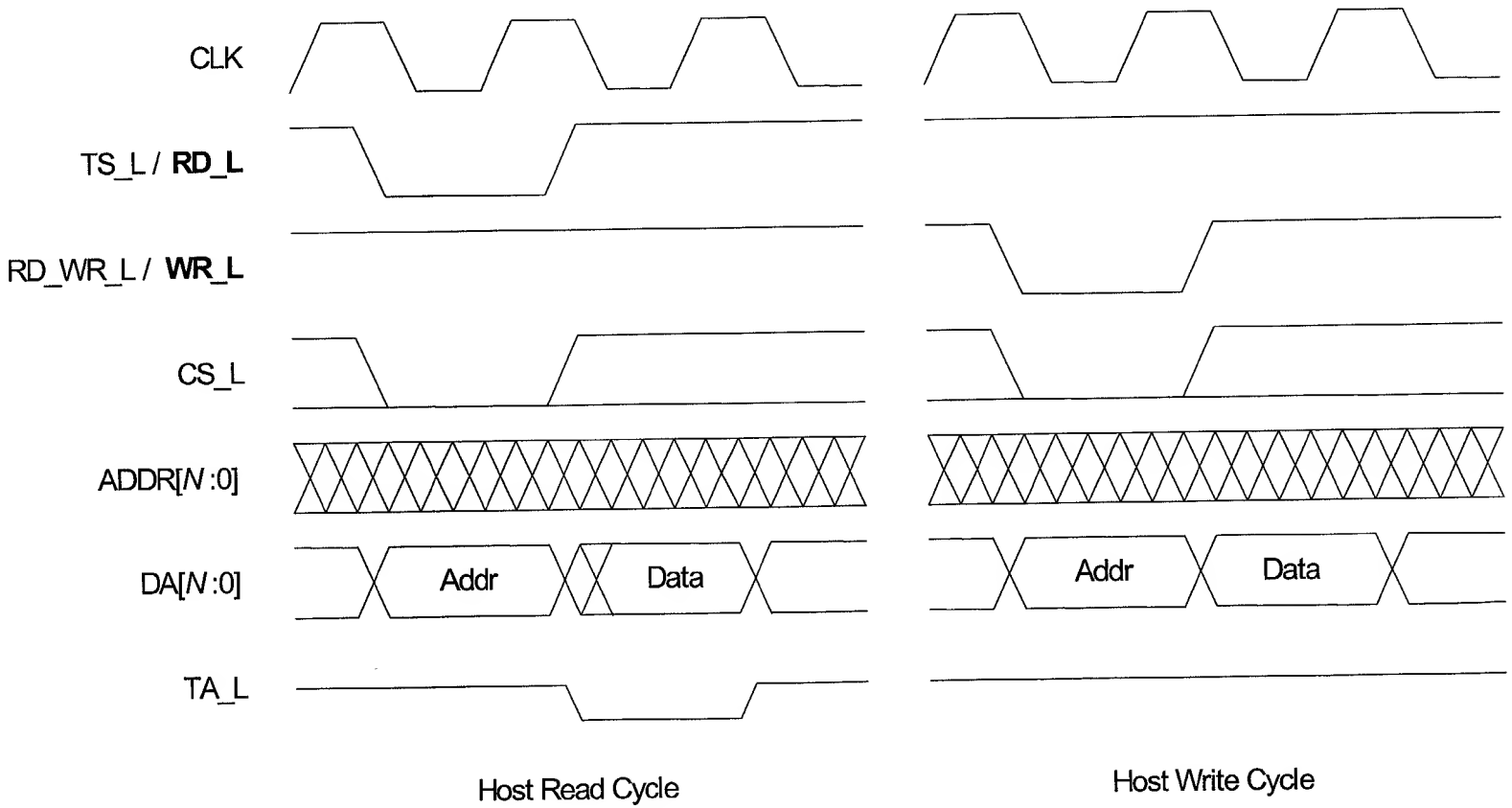

FIG. 6D

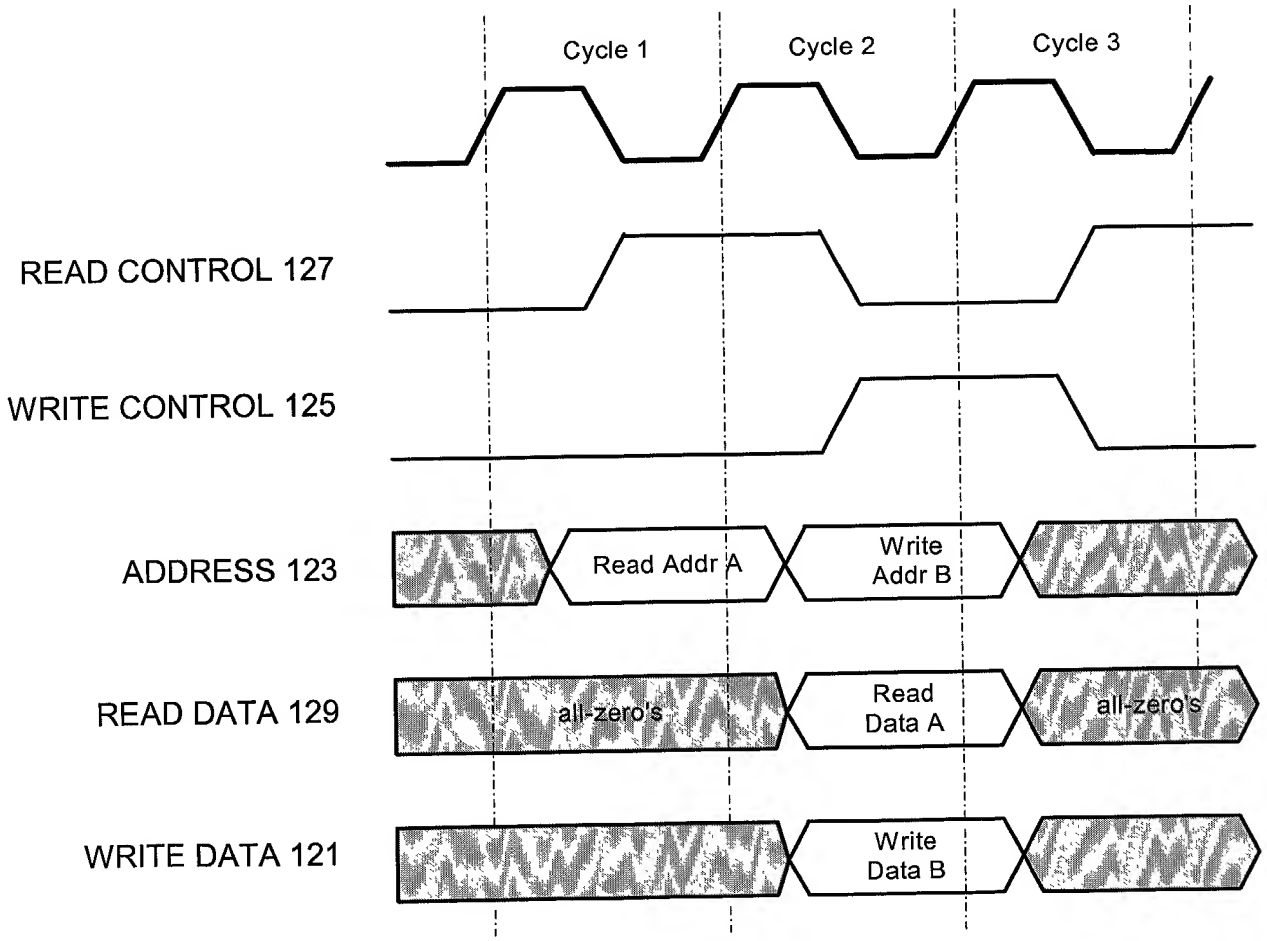
Cycle 1
Cycle 2
Cycle 3
READ CONTROL 127
WRITE CONTROL 125
ADDRESS 123
Read Addr A
Write Addr B
READ DATA 129
all-zero's
Read Data A
all-zero's
WRITE DATA 121
Write Data B

FIG. 7

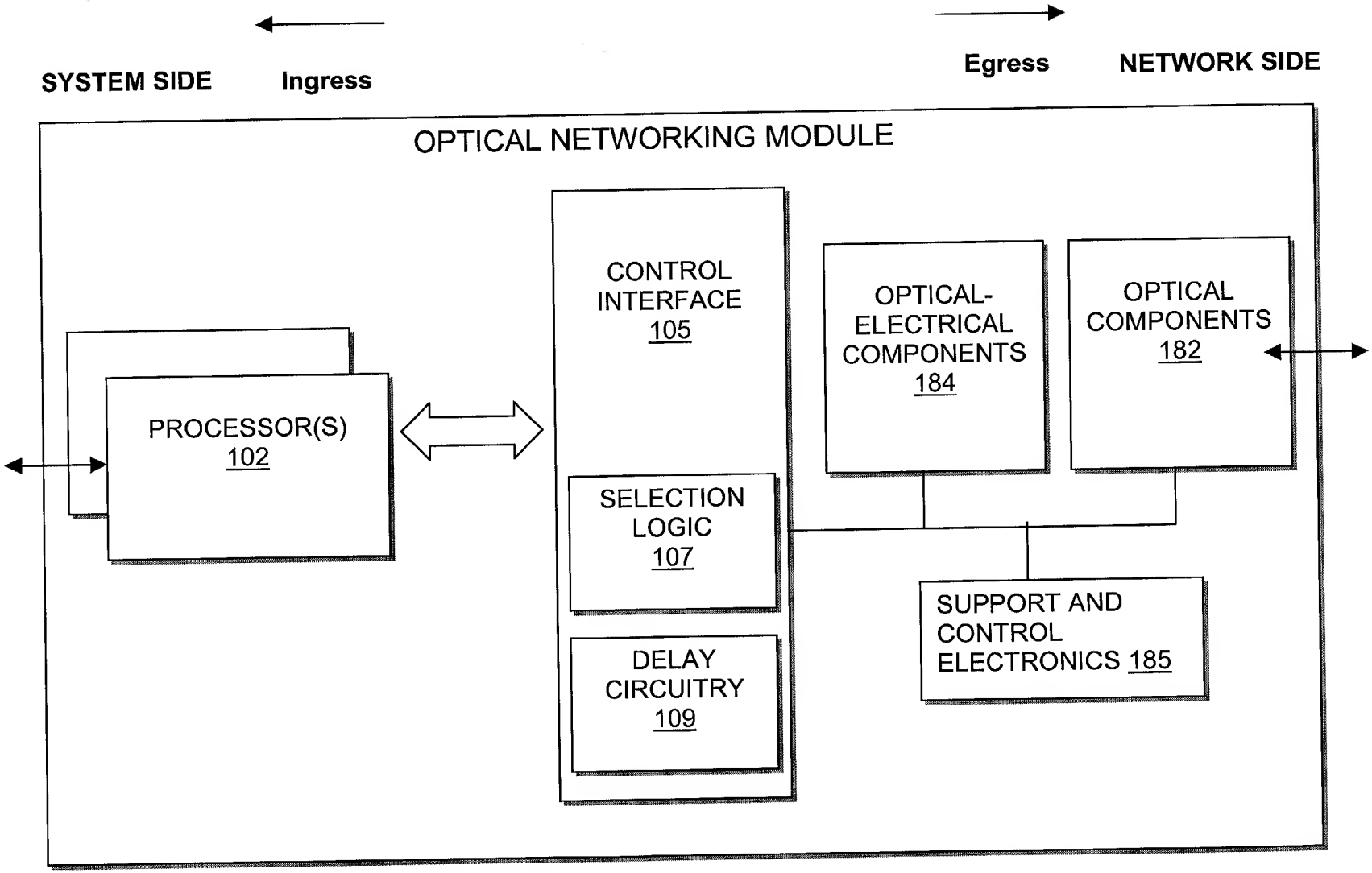
SYSTEM SIDE
Ingress
Egress
NETWORK SIDE
OPTICAL NETWORKING MODULE
PROCESSOR(S)
102
CONTROL
INTERFACE
105
SELECTION
LOGIC
107
DELAY
CIRCUITRY
109
OPTICAL-
ELECTRICAL
COMPONENTS
184
OPTICAL
COMPONENTS
182
SUPPORT AND
CONTROL
ELECTRONICS 185

FIG. 8

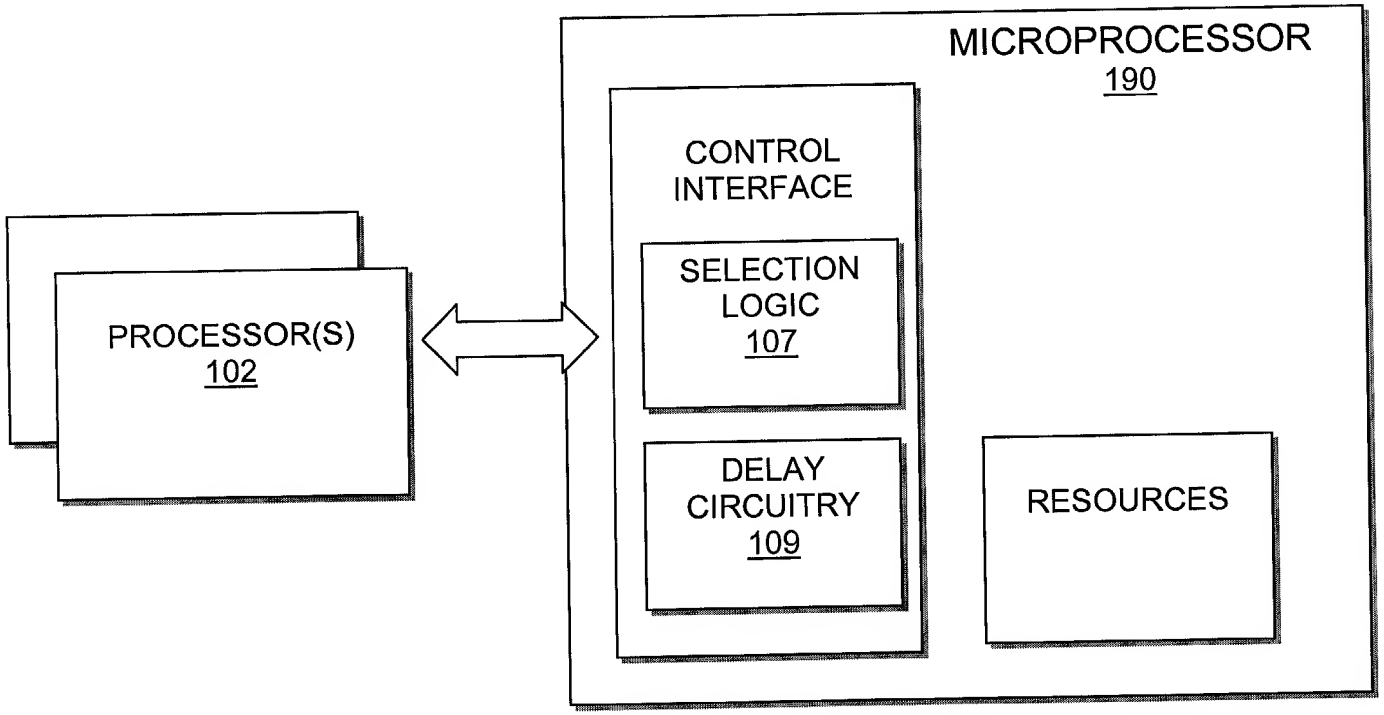
MICROPROCESSOR
190
CONTROL
INTERFACE
SELECTION
LOGIC
107
DELAY
CIRCUITRY
109
RESOURCES
PROCESSOR(S)
102

FIG. 9